COURSE DESCRIPTION CARD - SYLLABUS

Course name
Programmable Digital Circuits

Course

Field of study
Electronics and Telecommunications

Year/Semester
3/5

Area of study (specialization)

Profile of study
general academic

Level of study
Second-cycle studies

Course offered in
english

Form of study
full-time

Requirements
compulsory

Number of hours

Lecture	Laboratory classes	Other (e.g. online)
30	30	
Tutorials	**Projects/seminars**	
0	0	

Number of credit points

5

Lecturers

Responsible for the course/lecturer:
dr inż. Olgierd Stankiewicz,
olgierd.stankiewicz@put.poznan.pl

Responsible for the course/lecturer:

Prerequisites

Has Has a basic knowledge of Boolean algebra.
Has a knowledge in area of programming in C / C + +.
Has a general knowledge about combinational and sequential digital circuits.
Has a general knowledge in area of binary arithmetic and digital representation of signals.
Is able to look for information required during design process and take educational courses, if needed, especially through Internet and distance education.
Knows the limitations of their own knowledge and skills; can precisely formulate questions; understands the need for further education and systematic reading of scietnific journals in the field.
Can work individually and in team; knows the responsibility for tasked realized in team.

Course objective

The main purpose of the course is to show various design techniques for digital ciruits that can be suitable for ASIC/FPGA devices. As hardware description language the Verilog will be used. A lot of examples will show how to efficiently use all basic and generic FPGA blocks (like RAM, DSP, etc.).

Laboratory work will be performed with exploiting FPGA boards.

Course-related learning outcomes

Knowledge

Student has a basic skill in design of simple digital devices.
Student has a basic knowledge about the principle of operation of fast communication interfaces.
Student has a basic knowledge about designing a state machines.

Skills

Can describe complex digital system as a hierarchy of modules using Verilog language.
Can correctly determine the parameters of the interface between the two frequency domains.
Can acquire data from the literature and other sources, can integrate the information, make their interpretation, as well as formulate and to justify opinions.

Social competences

Can see and analyze development of design techniques.
Ability of self-learning (textbooks, computer programs).
Knowing the responsibility for the electronic and telecommunication systems being designed.

Methods for verifying learning outcomes and assessment criteria

Learning outcomes presented above are verified as follows:
Lecture: written exam
The written exam is a set of 6-10 problematic questions, for which desciptory answer is expected.
Each answer is ranked from 0 to 1 points (fractinal points also possible).
The exam is passed if the number of attained points is greater than 50%. More than 50% indicates the knowledge above of satisfactory level.
The course issues of which the questions are prepared, are sent to students by e-mail using the university's e-mail system.

Laboratories:
Activity during classes, reports from particular activities. Laboratory project realized individually/in small groups.

Programme content

Lecture:
Introduction to digital programmable devices. General structrue of FPGA devices. Basic embedded blocks (RAM, PLL, FIFO, etc.). Comparison of different FPGA devices. Inter-domain communication (source-synchronous interface). High-speed I/O interfaces - Use Gigabit GTP, GTX, GTH modules in HD-SDI, SATA, PCI-E, and SerDes. Systems in Layout (SoC). Programming languages - Verilog, SystemC, SystemVerilog, migen, MyHDL. Principles of good programming, self-describing code.

Methods and tools for simulation and synthesis of projects on FPGA devices - EDIF file generation, project partitioning, Python scripting language.

Examples of effective implementation of selected algorithms (DCT conversion, RGB-YUV colour space conversion, elementing, composite multiplication, floating point operations), for FPGA devices.

Laboratories:
Simulation and synthesis framework and software. Basic testbenches. Design of various modules: random number generators. binary coded decimals converter, buffer modules (e.g. stack, fifo), arithmetic logic units, state machines. Design of a system comprising state machines, e.g. demonstration of traffic lights, or equation calculator in infix/postfix notation.

Teaching methods

Lecture: multimedia presentation with examples presented on the blackboard.

Laboratories: work on computers with simulation and synthesis software. Usage of FPGA boards. Examples illustrated on screen/blackboard.

Bibliography

Basic
Skahill K., VHDL for Programmable Logic / Język VHDL , WNT, SBN-13: 978-0201895735, ISBN-10: 0201895730.
Giovanni De Micheli, Synthesis and Optimization of Digital Circuits / Synteza i optymalizacja układów cyfrowych , WNT, ISBN-13: 978-0070163331 ISBN-10: 0070163332.

Additional
Łuba T., Rawski M., Tomaszewicz P., Zbierzchowski B., Synteza układów cyfrowych, Wydawnictwa Komunikacji i Łączności, Warszawa 2003.
Hajduk Z., Wprowadzenie do języka Verilog, BTC, Warszawa 2009.
Kamionka-Mikuła H., Małysiak H., Pochopień B., Synteza i analiza układów cyfrowych, WKŁ.Zbysiński P., Pasierbiński J.: Układy programowalne pierwsze kroki, Wydawnictwo BTC, Warszawa 2004,
Łuba T.. : Synteza układów logicznych. Oficyna Wyd. PW, Warszawa, 2005.

Breakdown of average student's workload

	Hours	ECTS
Total workload	125	5,0
Classes requiring direct contact with the teacher	70	3,0
Student's own work (literature studies, preparation for laboratory classes, preparation for exam, laboratory project preparation) [1]	55	2,0

[1] delete or add other activities as appropriate